No. 06-1050.

Respectfully submitted,

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MARKED-UP VERSION OF THE AMENDED CLAIMS

4. (Amended) The pattern synchronous circuit as defined in claim 2 [or 3,] wherein

said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

5. (Amended) The pattern synchronous circuit as defined in claim 2 [or 3,] wherein

said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

6. (Amended) The pattern synchronous circuit as [in any one of claims 1 to 3] defined in claim 1, wherein

the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

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